Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S2	5814914	(FPGA circuit component LUT CLB)	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/20 13:14
S4	2501	S3 and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/20 13:16
S3	339886	S1 same S2	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/20 13:16
S6	116	S3 and "716"/$.ccls. and slice and @ad<"20030930"	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/20 13:17
S8	113	S3 and "716"/$.ccls. and slice and @ad<"20030930" and (connect$3 interconnect$3 rout$3) and (minimiz$5 alleviat$3 reduc$5 eliminat$4 optimiz$5)	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/20 13:21
S12	81	S3 and "716"/$.ccls. and slice and @ad<"20030930" and (connect$3 interconnect$3 rout$3) same (minimiz$5 alleviat$3 reduc$5 eliminat$4 optimiz$5)	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/20 13:47
S11	6	S3 and "716"/$.ccls. and slice and @ad<"20030930" and (critical)same(connect$3 interconnect$3 rout$3) near10 (minimiz$5 alleviat$3 reduc$5 eliminat$4 optimiz$5)	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/20 13:47
S1	1804814	(pack$3 cluster$3 partition$3)	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/20 14:01
S13	30	(pack$3 cluster$3 partition$3)same FPGA same slic$3	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/20 14:05
S16	44	(pack$3 cluster$3 partition$3)same slic$3 same (component subcircuit circuit LUT CLB lookup look-up configurable adj logic adj block)and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/20 14:08
S5	129	S3 and "716"/$.ccls. and slice	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/20 14:11

S18	45	S3 same slic$3 and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/20 14:12
S19	22	S3 same slic$3 same (connect$4 interconnect$4 wir$4 rout$3)and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/20 14:13
S23	116	S22 and "716"/$.ccls. and slice and @ad<"20030930" and (connect$3 interconnect$3 rout$3)	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/20 16:36
S22	339886	S20 same S21	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/20 16:36
S21	5814914	(FPGA circuit component LUT CLB)	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/20 16:36
S20	1804814	(pack$3 cluster$3 partition$3)	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/20 17:31
S26	93	(pack$3 cluster$3)same plac$5 same slic$3 same (connect$3 interconnect$3 inter-connect$3 rout$3 wiring path) same (alleviation minimiz$5 optimiz$5)	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/20 17:37
S28	234	(pack$3 cluster$3)same slic$3 same (connect$3 interconnect$3 inter-connect$3 rout$3 wiring path) same (alleviation minimiz$5 optimiz$5)	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/20 17:38
S29	1	(pack$3 cluster$3)same slic$3 same (connect$3 interconnect$3 inter-connect$3 rout$3 wiring path) same (alleviation minimiz$5 optimiz$5) and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/20 17:39
S32	3	pack$3 and cluster$3 and slic$3 same (connect$3 interconnect$3 inter-connect$3 rout$3 wiring path) same (alleviation minimiz$5 optimiz$5) and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/20 18:16
S33	44	pack$3 and cluster$3 and slic$3 and (connect$3 interconnect$3 inter-connect$3 rout$3 wiring path) near10 (alleviation minimiz$5 optimiz$5) and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/20 18:28

S35	44	pack$3 and cluster$4 and slic$3 and (initial prior) and (connect$3 interconnect$3 inter-connect$3 rout$3 wiring path) near10 (alleviation minimiz$5 optimiz$5) and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/20 18:29
S34	44	pack$3 and cluster$3 and slic$3 and (initial prior) and (connect$3 interconnect$3 inter-connect$3 rout$3 wiring path) near10 (alleviation minimiz$5 optimiz$5) and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/20 18:29
S38	945	(pack$3 partition$3 group$3) same (circuit component cell sub-circuit subcircuit portion sub-region subregion sub-area subarea) same cluster$3 same (connect43 interconnect$3 inter-connect$3 rout$3)	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/21 13:15
S42	2	(pack$3 partition$3 group$3) same (circuit component cell sub-circuit subcircuit portion sub-region subregion sub-area subarea) same cluster$3 same (critical slack delay timing constraint) same (connect43 interconnect$3 inter-connect$3 rout$3) same (minimiz$5 optimiz$5 reduc$4 alleviat$3) same (partition divid$3 packag$3) same (PLD FPGA) and architecture and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/21 15:40
S43	2	(pack$3 partition$3 group$3) same (circuit component cell sub-circuit subcircuit portion sub-region subregion sub-area subarea) same cluster$3 same (critical slack delay timing constraint) same (connect43 interconnect$3 inter-connect$3 rout$3) same (minimiz$5 optimiz$5 reduc$4 alleviat$3) same (partition divid$3 packag$3) and (PLD FPGA) and architecture and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/21 15:41
S45	591	(partition divid$3 packag$3 pack$3) and (PLD FPGA) and architecture and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/21 15:45

S44	4	(pack$3 partition$3 group$3) same (circuit component cell sub-circuit subcircuit portion sub-region subregion sub-area subarea) same cluster$3 same (critical slack delay timing constraint) same (connect43 interconnect$3 inter-connect$3 rout$3) same (minimiz$5 optimiz$5 reduc$4 alleviat$3) and (partition divid$3 packag$3 pack$3) and (PLD FPGA) and architecture and "716"/$. ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/21 15:45
S48	30	(partition divid$3 packag$3 pack$3) same(PLD FPGA) same architecture same (wir$3 path interconnect$3 connection)and "716"/$.ccls. and @ad<"20030930"	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/21 15:48
S47	60	(partition divid$3 packag$3 pack$3) same(PLD FPGA) same architecture and "716"/$.ccls. and @ad<"20030930"	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/21 16:58
S51	3	(partition divid$3 packag$3 pack$3) same(PLD FPGA) same (input near4 (threshold constraint)) and "716"/$. ccls. and @ad<"20030930"	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/21 17:00
S41	22	(pack$3 partition$3 group$3) same (circuit component cell sub-circuit subcircuit portion sub-region subregion sub-area subarea) same cluster$3 same (critical slack delay timing constraint) same (connect43 interconnect$3 inter-connect$3 rout$3) same (minimiz$5 optimiz$5 reduc$4 alleviat$3) and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/21 17:02
S53	9	(pack$3 partition$3 group$3 packag$3) same (circuit component cell sub-circuit subcircuit portion sub-region subregion sub-area subarea) same cluster$3 same (critical slack delay timing constraint) same (connect43 interconnect$3 inter-connect$3 rout$3 pin) same (minimiz$5 optimiz$5 reduc$4 alleviat$3) and (PLD or FPGA) and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/21 17:07

S52	8	(pack$3 partition$3 group$3 packag$3) same (circuit component cell sub-circuit subcircuit portion sub-region subregion sub-area subarea) same cluster$3 same (critical slack delay timing constraint) same (connect43 interconnect$3 inter-connect$3 rout$3) same (minimiz$5 optimiz$5 reduc$4 alleviat$3) and (PLD or FPGA) and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/21 17:07
S46	66	(partition divid$3 packag$3 pack$3) same(PLD FPGA) same architecture and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/21 17:14
S62	0	(pack$3) same (FPGA or PLD) same cluster$3 same(architecture near4 circuit) and "716"/$.ccls. and @ad<"20030930"	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/22 09:21
S63	1	(pack$3) same (FPGA or PLD) same cluster$3 same(architecture near10 circuit) and "716"/$.ccls. and @ad<"20030930"	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/22 09:22
S65	10	(pack$3 partition$3 divid$3 packag$3) same (FPGA or PLD) same cluster$3 same(architecture) and "716"/$.ccls. and @ad<"20030930"	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/22 09:28
S68	1	(pack$3 partition$3 divid$3 packag$3) same (FPGA or PLD) and cluster$3 and(architecture near4 circuit) and (routing near4 driven) and "716"/$. ccls. and @ad<"20030930"	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/22 09:35
S67	0	(pack$3 partition$3 divid$3 packag$3) same (FPGA or PLD) and cluster$3 and(architecture near4 circuit) and (routing adj2 driven) and "716"/$. ccls. and @ad<"20030930"	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/22 09:35
S66	26	(pack$3 partition$3 divid$3 packag$3) same (FPGA or PLD) and cluster$3 and(architecture near4 circuit) and "716"/$.ccls. and @ad<"20030930"	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/22 09:48
S69	58	(pack$3 partition$3 divid$3 packag$3) same (FPGA or PLD) and (architecture near4 circuit) and "716"/$.ccls. and @ad<"20030930"	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/22 12:19
S73	1	(pack$3) same (FPGA or PLD) same cluster$3 same (maximum maxim$7 minimiz$7 less more greater larger)same(number threshold constraint) and "716"/$.ccls. and @ad<"20030930"	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/22 12:34

S74	10	(FPGA or PLD) same cluster$3 same (maximum maxim$7 minimiz$7 less more greater larger)same(number threshold constraint) and "716"/$.ccls. and @ad<"20030930"	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/22 12:35
S81	4673	(FPGA PLD) same pin same packing smae CLB	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/26 17:11
S82	8	(FPGA PLD) same pin same packing sameCLB	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/26 17:12
S86	927	(FPGA PLD) same (input output pin) same (cluster$3 pack$3)	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/26 17:17
S85	21	(FPGA PLD) same (input output pin) same packing	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/26 17:17
S88	22	(FPGA PLD) same (input output pin) same (cluster$3) and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/26 17:23
S91	1	(FPGA PLD) same (number near4(input output pin)) same (cluster$3) same (more less exceed)and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/26 17:28
S90	10	(FPGA PLD) same (input output pin) same (cluster$3) same (more less exceed)and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/26 17:29
S94	7	(FPGA PLD) same number same(input output pin) same (cluster$3 packing) same (more less exceed) and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/26 17:30
S87	114	(FPGA PLD) same (input output pin) same (cluster$3 pack$3) and "716"/$. ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/26 19:52
S98	7	CLB same (more less exceed) same (input output pin) same (cluster$3 pack$3) and "716"/$.ccls. and @ad<"20030901"	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/26 19:59
S99	10	CLB same (more less exceed) same (input output pin) same (cluster$3 pack$3 map$4) and "716"/$.ccls. and @ad<"20030901"	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/27 08:22

S97	32	CLB same (input output pin) same (cluster$3 pack$3) and "716"/$.ccls. and @ad<"20030901"	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/27 08:40
S101	72	CLB same (input output pin) same (cluster$3 pack$3 partition$3 map$4 group$3) and "716"/$.ccls. and @ad<"20030901"	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/27 08:46
S102	35	(CLB near5 (input output pin)) same (cluster$3 pack$3 partition$3 map$4 group$3) and "716"/$.ccls. and @ad<"20030901"	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/27 09:44
S107	12	(CLB near5 (input output pin terminal connect$3 interconnect$3)) same (cluster$3 pack$3 partition$3 map$4 group$3) and (Rent rule) and "716"/$.ccls. and @ad<"20030901"	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/27 09:48
S100	6	CLB same (more less exceed) same number same (input output pin) same (cluster$3 pack$3 map$4 partition$3) and "716"/$.ccls. and @ad<"20030901"	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/28 13:53
L2	66	(CLB FPGA PLD) same (more less exceed) same (capacity number) same (input output pin interconnect$3 connect$3 terminal) same (decluster$3 cluster$3 pack$3 map$4 partition$3)and "716"/$.ccls. and @ad<"20030901"	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/28 14:01
L1	0	(CLB FPGA PLD) same (more less exceed) same (capacity number) same (input output pin interconnect$3 connect$3 terminal) same (decluster$3 cluster$3 pack$3 map$4 partition$3)same ((unused white ("not" adj2 used)) near4 (space area portion routing resource))and "716"/$.ccls. and @ad<"20030901"	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/28 14:01
L4	2	L2 and L3	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/28 14:04
L3	15	CLB same (unused white ("not" adj2 used)) same (space area portion routing resource) and (post-placement placement) and "716"/$.ccls. and @ad<"20030901"	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/28 14:04
L5	1	(pack$3 partition$3 divid$3 packag$3) same (FPGA or PLD) same cluster$3 same(architecture near10 circuit) and "716"/$.ccls. and @ad<"20030930"	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/28 14:18